Vertical Enhancement-Mode InAs Nanowire Field-Effect Transistor With 50-nm Wrap Gate

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***Abstract*—We present results on fabrication and dc characterization of vertical InAs nanowire wrap-gate field-effect transistor arrays with a gate length of 50 nm. The wrap gate is defined by evaporation of 50-nm Cr onto a 10-nm-thick HfO_2 gate dielectric, where the gate is also separated from the source contact with a 100-nm SiO_x spacer layer. For a drain voltage of 0.5 V, we observe a normalized transconductance of 0.5 S/mm, a subthreshold slope around 90 mV/dec, and a threshold voltage just above 0 V. The highest observed normalized on current is 0.2 A/mm, with an off current of 0.2 mA/mm. These devices show a considerable improvement compared to previously reported vertical InAs devices with SiN_x gate dielectrics.**

***Index Terms*—Field-effect transistor (FET), InAs, nanowires.**

I. Introduction

DEVELOPMENT of lithographic techniques has given access to shorter gate lengths in transistor processing, and thus, higher possible switching frequencies. However, the aggressive scaling of the gate length comes at the expense of control of the charges in the transistor channel. As a consequence, short-channel effects such as high off currents and poor subthreshold slopes are becoming problematic. The design of the field-effect transistors (FETs) is therefore rapidly moving toward the use of high-κ dielectrics and geometries, where the gate partially, or fully, wraps around the transistor channel [1]. In addition, there is a strong interest in introducing III–V channels to boost the drive current.

Wrap-gate FETs show the possibility of high scalability [2], and the concept has recently been demonstrated with both lateral and vertical channel geometries. Suk *et al.* have shown transistor data for 10-nm lateral Si wires with a full wrap gate using SiO_2 as gate dielectric [3]. In the vertical geometry, many groups are currently working with epitaxially grown nanowires [4]–[7]. An important motivation here is the possibility of growing group III–V nanowires directly on Si, as well as highly lattice-mismatched semiconductor heterostructures within a wire [8]–[10]. Successful integration of vertical nanowires as active element in transistors may offer considerable improvement in device performance and may also give rise to new device concepts. Engineering of the band structure in a nanowire could improve breakdown voltages, give rise to higher mobilities, and substantially reduce power consumption by lowering the drive voltage. However, postgrowth processing on vertical wires is challenging as they are less mechanically stable than their lateral counterparts, and it is difficult to accurately control the vertical position and length of a wrap gate and the surrounding dielectric layers. Moreover, doping is not fully understood for nanowires, and radio frequency-compatible devices have not yet been realized.

In this letter, we report on fabrication of vertical wrap-gate FETs based on InAs nanowires with an average diameter of 50 nm. The length of the wrap gate is set by the thickness of the evaporated Cr (50 nm), which means that the process is scalable to shorter gate lengths. The Cr layer is separated from the nanowire channel by a 10-nm-thick HfO_2 gate dielectric and from the source contact with 100-nm SiO_x. We observe a considerable improvement in on/off current ratio $(I_{\mathrm{ON}}/I_{\mathrm{OFF}})$ and maximum transconductance g_m compared to previous work, where Au/SiN_x was used as gate metal/dielectric [11].

II. Nanowire Growth and Processing

Arrays of nanowires are obtained by first fabricating ordered Au seeds by electron-beam lithography and metal evaporation/liftoff of Au onto InAs $\langle 111 \rangle$B substrates. Each sample has 120 arrays, with various selected seed diameters and array sizes. InAs nanowires are grown by chemical beam epitaxy at a temperature of 425 °C, using trimethylindium and tertiarybutylarsine as precursors. During the last stage of the growth, the sample is also exposed to ditertiarybutylselenium, which results in n-type (Se) doping of the top segment of the wires. An example of the largest array, having 91 nanowires, is shown in Fig. 1(a). The diameter spread was rather large for the sample studied here, around 50 $\pm$ 10 nm, which is mainly caused by uncompensated proximity effects in the electron-beam exposure.

The first processing step after growth is deposition of 5-nm HfO_2 by atomic layer deposition (ALD) at 250 °C, using tetrakis (dimethylamido)hafnium(IV) and H_2O as precursors. This is followed by tilted evaporation of 100-nm SiO_x with the samples rotating. The purpose of the SiO_x layer is to lift the gate layer from the substrate. Excess SiO_x, which is deposited onto the sides of the nanowires, is removed with hydrogen fluoride (HF). This is followed by ALD of another 5-nm HfO_2; the total thickness of the HfO_2 gate dielectric is thus 10 nm.

A gate-metal layer is deposited by tilted evaporation of 50-nm Cr onto rotating samples. This gives a high precision

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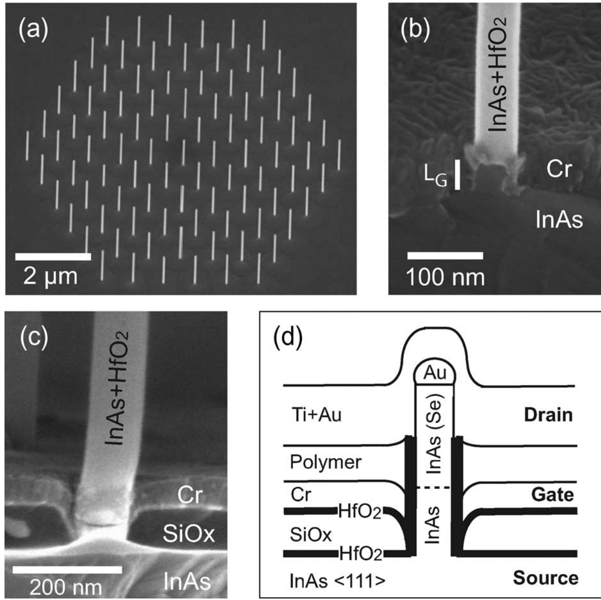

Fig. 1. (a) Array of InAs nanowires on InAs. (b) Cleaved test sample, which shows that the thickness of the Cr gate layer around the base of the nanowire is around 50 nm (52° tilt). (c) Side view of a cleaved test sample where a (dark) SiO_x layer lifts the gate pad from the InAs source contact. (d) Schematic side view of the device.

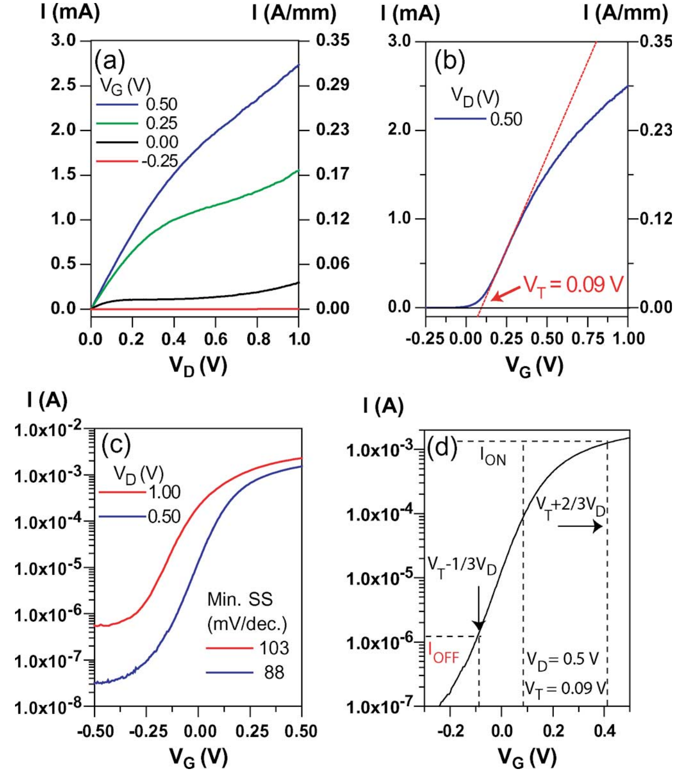

Fig. 2. Data in (a)–(d) were obtained for a nanowire array with nominally 61 nanowires (yield $\sim$90% estimated from scanning electron microscopy inspection after the measurements) and diameters around 50 nm. (a) Output characteristics for different wrap-gate voltages. (b) Transfer characteristics for $V_D = 0.50$ V. (c) Transfer characteristics plotted in a logarithmic scale for $V_D = 0.50$ and 1.0 V. (d) Extraction of I_{ON} and I_{OFF} using the metrics defined in [12].

in the resulting gate length. Excess material on the sides of the nanowires is removed by a short selective Cr etch. Fig. 1(b) shows the gate after removal of the side deposits for a cleaved test sample without the SiO_x source–gate spacer layer. The brighter contrast around the wire in Fig. 1(b) corresponds to the 10-nm-thick HfO_2. When the sample was cleaved, the Cr removed the HfO_2 with which it was in contact. This reveals the effective nanowire gate length L_G, which in Fig. 1(b) is 50 nm. Fig. 1(c) shows another cleaved test sample, in this case with a SiO_x spacer layer. It should be pointed out that both the SiO_x and the Cr layers have downslopes close to the wire base in this case. Gate pads are formed from the Cr layer by resist deposition, ultraviolet (UV) lithography, Cr etching in HCl, and resist removal.

An organic insulating layer based on a cross-polymerized photoresist is used as gate–drain separation. A gate-via is first formed with UV lithography, and the resist is then cured and dry-etched to a desired thickness using oxygen plasma. Typically, the gate–drain separation is 100–200 nm, depending on the time used for etch back. The polymer layer is used as an etch mask when removing the HfO_2 from the top of the nanowires in buffered HF. The sample is then exposed to diluted NH_4S_x, and a thick Ti/Au layer is evaporated with the sample rotating with a large tilt angle. Finally, the drain and gate pads are formed by resist coating, optical lithography, and wet etching. Fig. 1(d) shows a schematic side view of the device.

III. DC Characterization

Electrical measurements [Fig. 2(a)–(d)] are carried out using a probe station, where the InAs substrate acts as a source, the intermediate metal layer in Fig. 1(d) connects to the wrap gate, and the upper metal contact acts as a drain. The transistors operate as n-type MISFET accumulation devices, where a positive gate voltage leads to an increased carrier concentration in the channel. The threshold voltage V_T is extracted by a linear extrapolation from the point of the highest transconductance [Figs. 2(b) and 3(a)]. V_T is very close to 0 V for most devices and shows a shift in V_D (drain-induced barrier lowering) of approximately 60 mV/V for V_D between 0.10 and 0.70 V.

The average subthreshold slope minimum is around 100 mV/dec $(V_D = 0.50\ \mathrm{V})$ and shows a small dependence on V_D between 0.10 and 0.70 V. However, at $V_D = 1.0$ V, the minimum slope value has substantially increased for most arrays [Fig. 2(c)]. For $V_D = 0.50$ V and a V_G swing of 0.50 V, we observe $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratios around 10^3 (I_{ON} obtained at $V_G = V_T + 2/3V_D$ and I_{OFF} obtained at $V_G = V_T - 1/3V_D$ in accordance with the metrics defined in [12]) [Fig. 2(d)]. The highest observed normalized g_m is 0.52 S/mm for $V_D = 0.50$ V, and 0.80 S/mm at $V_D = 1.0$ V [Fig. 3(a) and (b)], where the values have been normalized by the total nanowire circumference and also adjusted for missing wires. It should be noted that the g_m values we report here, for large arrays of wires with a 50-nm gate length (0.80 S/mm), are comparable to previously reported values for individual InAs wires with a 2-μm gate length, taking into consideration a difference in π in the definition of gate width [13].

In arrays with very few and thin wires, it is possible to find minimum values of the subthreshold slope approaching the limit of 60 mV/dec. However, such low values come at the

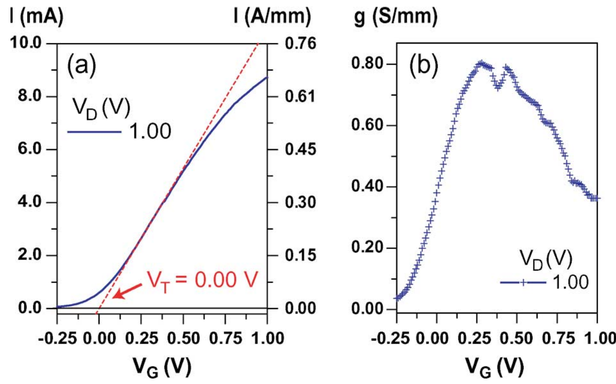

Fig. 3. (a) Transfer characteristics at $V_D = 1.0$ V for an array with nominally 91 wires (yield ∼90%). (b) Normalized transconductance plotted as a function of V_G.

TABLE I
DATA FOR NANOWIRE ARRAYS WITH WIRE DIAMETERS AROUND 50 nm. THE VALUES FOR g_m HAVE BEEN NORMALIZED TO THE TOTAL NANOWIRE CIRCUMFERENCE AND ALSO COMPENSATED FOR MISSING WIRES. STANDARD DEVIATION IS SHOWN FOR THE AVERAGED DATA. SS: SUBTHRESHOLD SLOPE

V_D (V)	V_T (V)	g_m (S/mm)	*Max.* g_m (S/mm)	*SS* (mV/dec.)	Min. *SS* (mV/dec.)
0.50	0.05 ± 0.05	0.44 ± 0.06	0.52	100 ± 8	88
1.00	0.00 ± 0.04	0.58 ± 0.12	0.80	150 ± 43	103

expense of a low g_m, which probably is a result of a large series resistance due to the small diameter at the source- and drain-side.

Overall, we observe gate leakage currents on the order of picoamperes, which correspond to a current density of 10^{-4} A/cm^2 for the vertical gate–nanowire interface. The hysteresis in the drain current for V_G sweeps from -0.50 to 0.50 V is about 20 mV. However, it increases as the gate voltage is swept to more negative values than -0.50 V, which indicates a threshold voltage for charge trapping; for sweeps to $V_G = -1.0$ V, the hysteresis has increased to around 200 mV.

It is important to note that some figures-of-merit for the devices, such as the subthreshold slope and the I_{ON}/I_{OFF} ratio, can become very poor even if only one individual wire in a 91-wire array has a failed wrap gate. Still, we observe surprisingly uniform values, indicating that the processing is stable over a large area of the sample and within the arrays. In Table I, averaged data are shown for nine functional nanowire arrays with wire diameters around 50 nm. The total number of wires included in the study is more than 700.

IV. CONCLUSION

A fabrication process has been developed for the formation of wrap gates to InAs nanowires with a gate length of only 50 nm, where HfO_2 is used as a gate dielectric. The I_{ON}/I_{OFF} ratio is around 10^3, and the minimum subthreshold slope is, on average, 100 mV/dec. We observe normalized g_m values up to 0.80 S/mm for $V_D = 1.0$ V, which is comparable to what has been reported in literature for lateral InAs wires with a much longer gate length. Since the vertical wrap-gate formation reported here is made by metal evaporation, we expect that we would be able to further scale the gate length.

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